

EQUIP: Error Correction for Quantum Information Processing

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Description

The last years have seen significant advances in the field of quantum technologies, consolidating the development of basic requirements for quantum computation. Protecting the quantum computation from noise and decoherence has become more topical than ever, challenging and bringing quantum error correction fairly close to the integration into practical quantum computers. To make such an integration viable, EQUIP aims at

- 1) providing radically new solutions to fault tolerant quantum computation, covering both intermediate and large-scale quantum systems, and
- 2) bridging the critical gap between algorithmic solutions and latency-power-scalability constrained hardware designs.

The project brings together interdisciplinary expertise, extending from the computer science foundations of quantum error correction and fault-tolerant computation, to algorithmic aspects, computer architectures, and HW designs.

Main Contributions

The main contributions of the proposed research are as follows.

- 1) Optimised low-qubit overhead solutions, suited but not restricted to intermediate scale quantum systems, including application-aware and software-based error mitigation techniques, and flag error correction protocols.
- 2) New approaches to accurate and hardware friendly decoding of quantum low-density parity-check codes, suited for large-scale systems, as well as alternative, disruptive approaches to fault-tolerant quantum computing, relying on quantum polar codes.
- 3) Demonstration of the effectiveness of the proposed solutions, through either their implementation into real intermediate-scale quantum devices and quantum simulators, or the hardware prototyping of the most promising decoding solutions for large-scale devices.

Project Details

Area of research: QPR / Quantum Computing

Project Duration: June 2022 – May 2025

Consortium:

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Funding Organizations: ANR (France), DFG (Germany), AEI (Spain), AKA (Finland)

Quantum Error Mitigation & Correction for NISQ Technology

- Software-based quantum error mitigation techniques
- Application-aware quantum error mitigation
- Low qubit overhead QEC using flag qubits

Quantum Error Correction for Large Scale Technology

- Message passing decoders for quantum LDPC codes
- Neural network based decoding solutions
- Polar codes for fault-tolerant quantum computation

Proof of Concept, Validation, and Evaluation

- Implementation of QEM/QEC solutions in NISQ devices
- Hardware prototyping of QEC decoders for large scale technology

Software-based quantum error mitigation techniques

- Trade-offs of quantum HW aware compilation techniques, including mapping and scheduling, and optimization of error mitigations solutions.
- SW/compilation framework, including the definition of performance metrics and an overall cost function or figure of merit, and incorporating different error mitigation techniques.

Application-aware quantum error mitigation

- Promising applications for NISQ and effects of different errors on their performance. Selection of algorithms for proof of concept experiments.
- Improvement of the SW-based error mitigation techniques, by adapting the software according to the quantum algorithm's properties.

Low qubit overhead QEC using flag qubits

- Methodology for efficiently implementing low-qubit overhead QEC protocols on resource-constrained quantum processors, using graph embedding techniques for their mapping and circuit optimization.
- Cross-stack approach, using flag qubits to extract flag information from the high-level circuit, to augment error-correction capabilities.
- Performance of QEC codes with flag qubits in the presence of biased noise and for HW-inspired error models.

Implementation of QEM/QEC solutions in NISQ devices

- Adapt the most efficient compilation techniques developed for a target quantum hardware in which experiments will be run e.g., HW platforms made available by IBM, the OpenSuperQ and the Finnish IQM projects).
- Prototypically implement: a) a software feedback loop for the experiments to run close to real-time; b) software circuit simulations with efficient sampling capabilities, coupled to the correction and mitigation solutions.

Iterative message passing decoders for quantum LDPC codes

- General purpose MP-based decoding algorithms for quantum LDPC codes, suitable for high-speed, low-power, scalable implementations.
- Optimizing novel decoding rules, able to cope with the code degeneracy, using insights provided by quantum trapping sets.
- Novel simplifications and optimizations of iterative decoding algorithms, including message passing and small set flip based approaches.

Development of neural-network based decoding solutions

- NN-based decoders and diversity architectures, handling code degeneracy, in a manner that is scalable with respect to decoding and training.
- HW-convenient NN-based decoders, e.g., that can be mapped back to MP decoding algorithms, suitable for later hardware implementations and meeting the constraints of the quantum system.

Polar codes for fault-tolerant quantum computation

- Framework of fault-tolerant quantum computation using quantum polar codes, incorporating fault-tolerant procedures for logic state preparation, error syndrome extraction, and a universal set of logic gates.
- Optimized mappings onto connectivity-constrained architectures, so as to minimize the number and extent of distant operations.

HW prototyping of QEC decoders for large scale technology

- Design hardware architectures for the proposed decoding algorithms, which can be flexibly adapted to different quantum LDPC codes.
- Explore different FPGA design frameworks, so as to a) find the most suitable workflow to meet the quantum technology constraints, and b) simplify the changes in the hardware when either the structure or the decoding rules of the QEC need to be updated.

