SIQUOS
Superconducting Silicon Qubit in CMOS Technology

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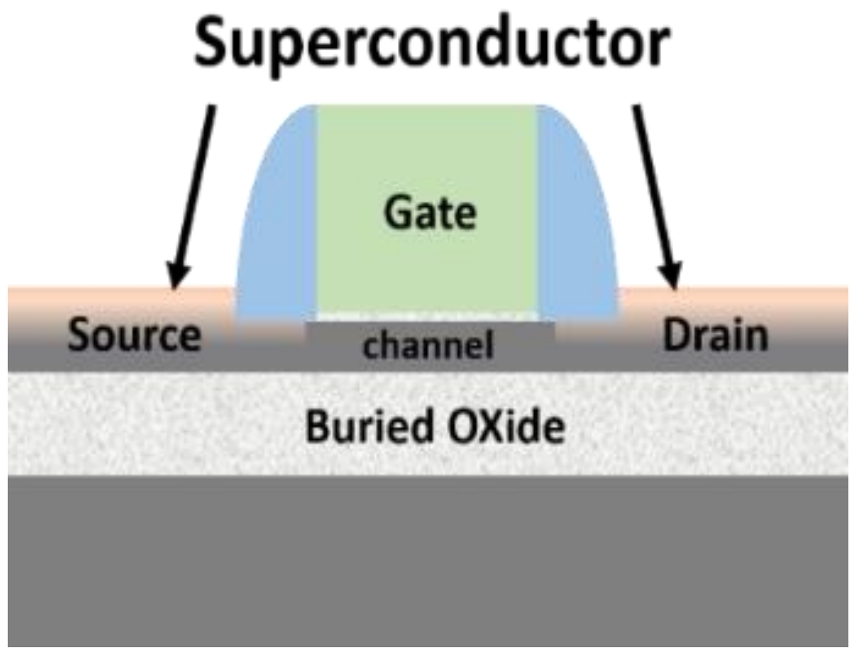
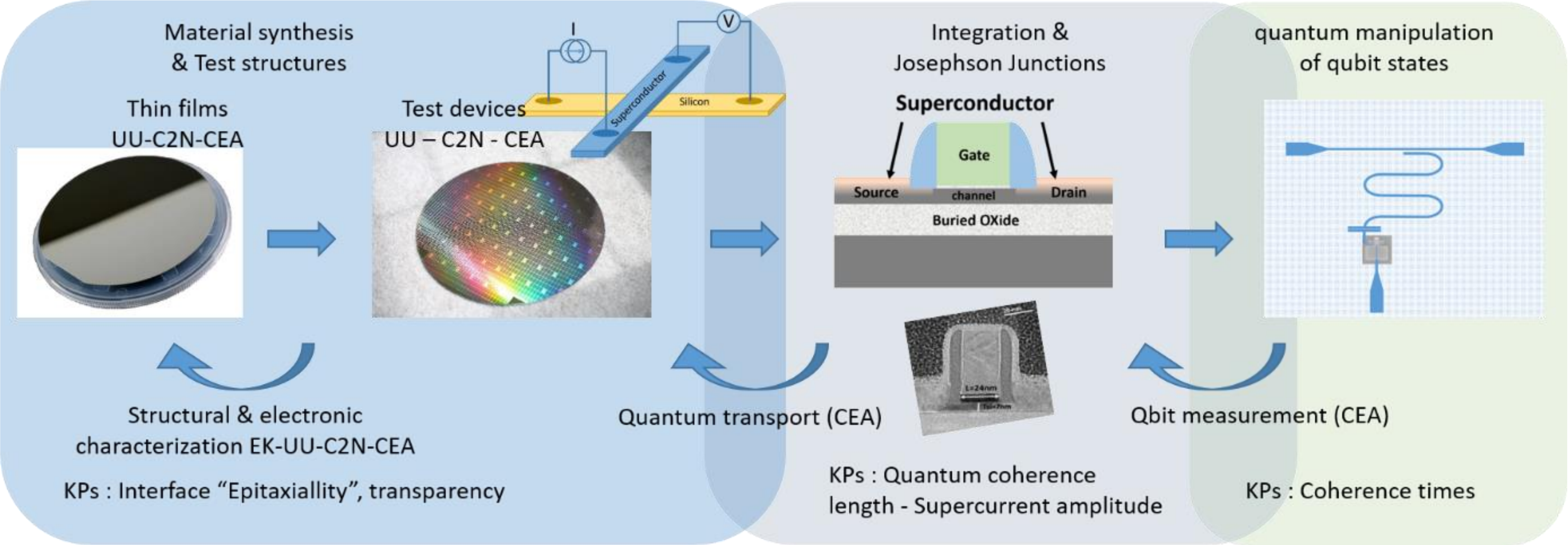


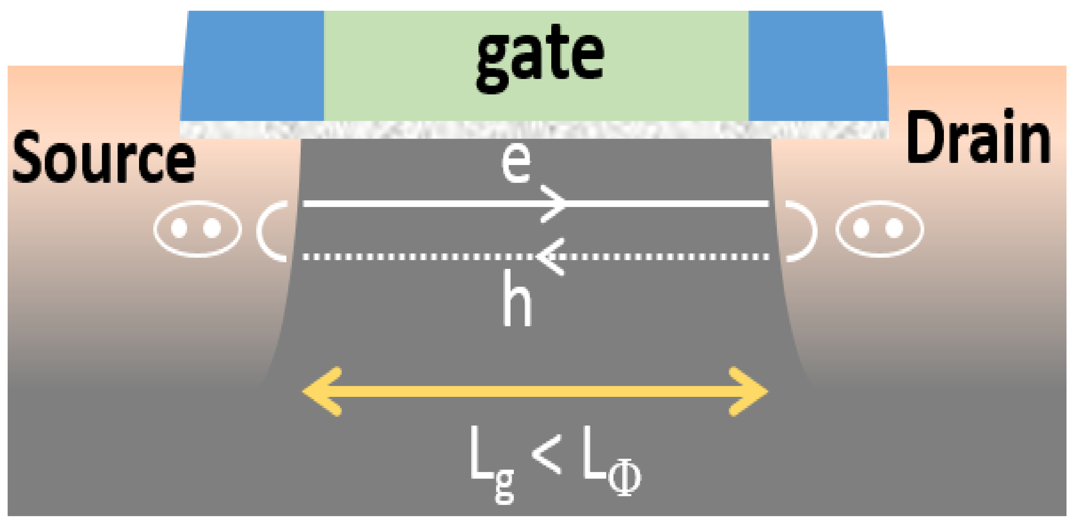
The aim of SIQUOS is to realise and study a **Si gatemon qubit, a gate tuneable transmon qubit composed of a Si Josephson field-effect transistor (JoFET)** coupled to a microwave resonator. It represents a valid integrable and scalable alternative to fully metallic superconducting qubits.
SIQUOS will focus on the **Si JoFET, i.e., a Si transistor with superconducting source and drain (S&D) contacts**, whose non-dissipative supercurrent can be modulated by an electrostatic gate. **CMOS-compatible metal silicides or heavily boron (B) doped Si will be used as the superconducting S&D contacts**. A comprehensive investigation of the superconductor/Si (S/Sm) interface by means of structural, chemical and low-temperature electronic transport characterisation will be performed. The first and foremost objective of SIQUOS is to **optimise the S/Sm interface transparency** so as to allow for the transfer of correlated charge carriers from the superconducting contacts into the Si channel and to reach large, reproducible supercurrents. The second objective is to realise Si JoFETs, demonstrating the gate tuneability of the Josephson supercurrent. Thereupon, the third and final objective is to integrate Si JoFETs in a transmon geometry including on-chip capacitors and resonators, and to realise the manipulation of quantum states in Si-gatemon devices.

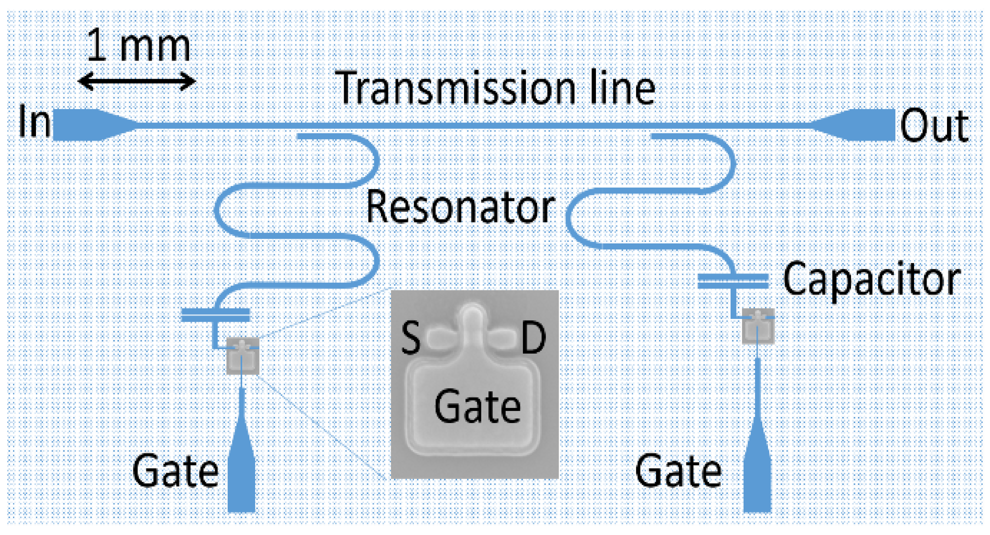


Requirements

- Gate tuneability
- Short gate length ($L_g \approx 50 – 100$ nm)
- Superconducting S/D contacts
- Low contact resistance ($R_c \approx 10^{-9}\ \Omega\ cm^2$)
- On-chip resonators $Q \approx 10^3$

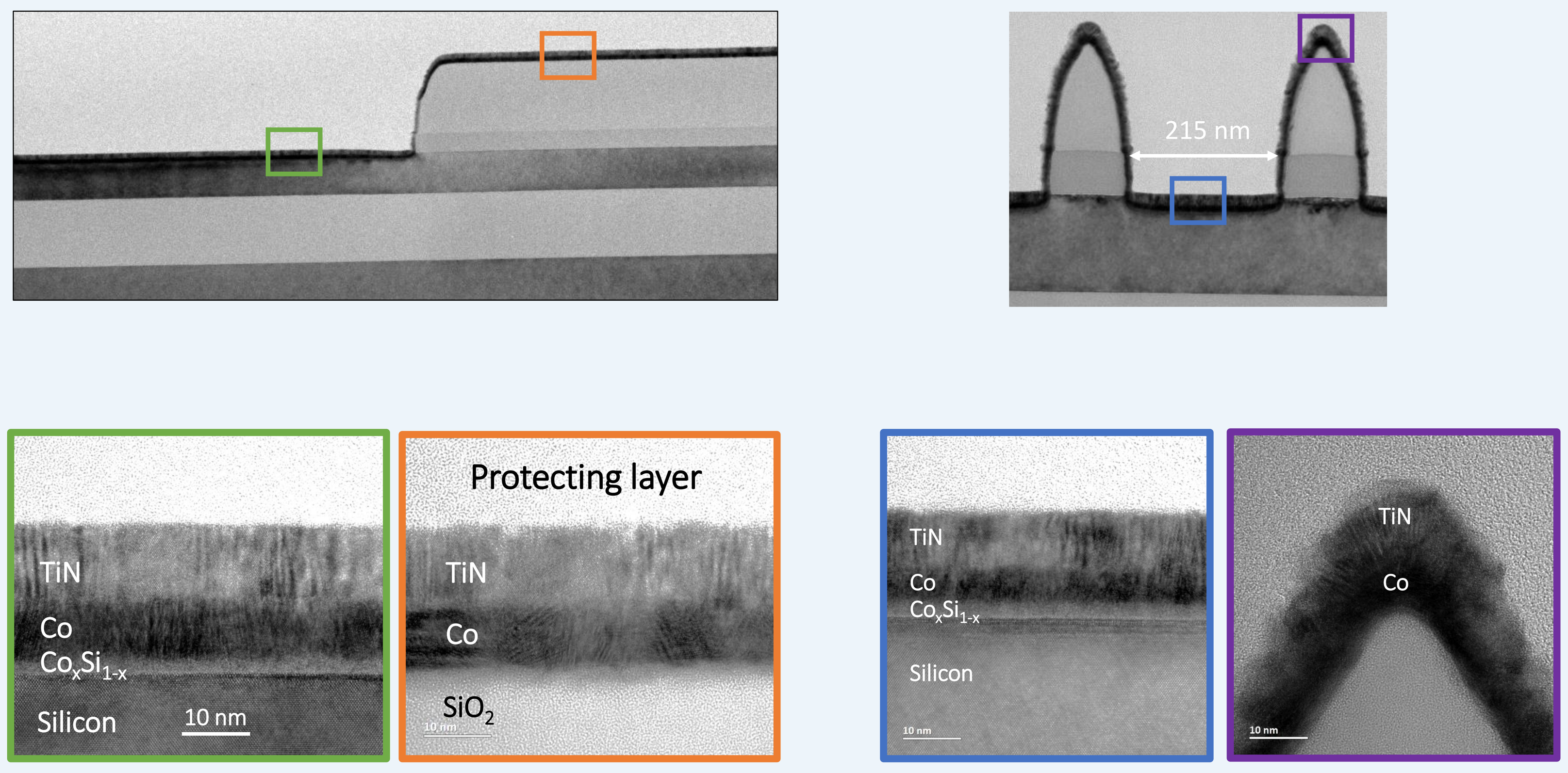
From a JoFET to a superconducting gatemon qubit …





Silicide : $CoSi_2$

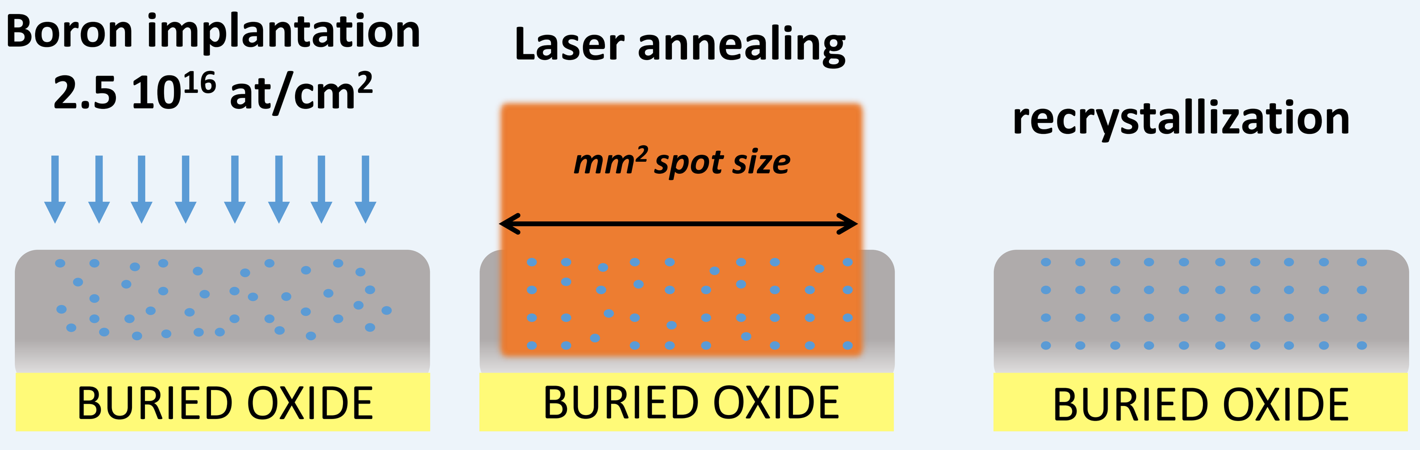
→ Study of deposition of Co and TiN cap layer on pre-patterned structures

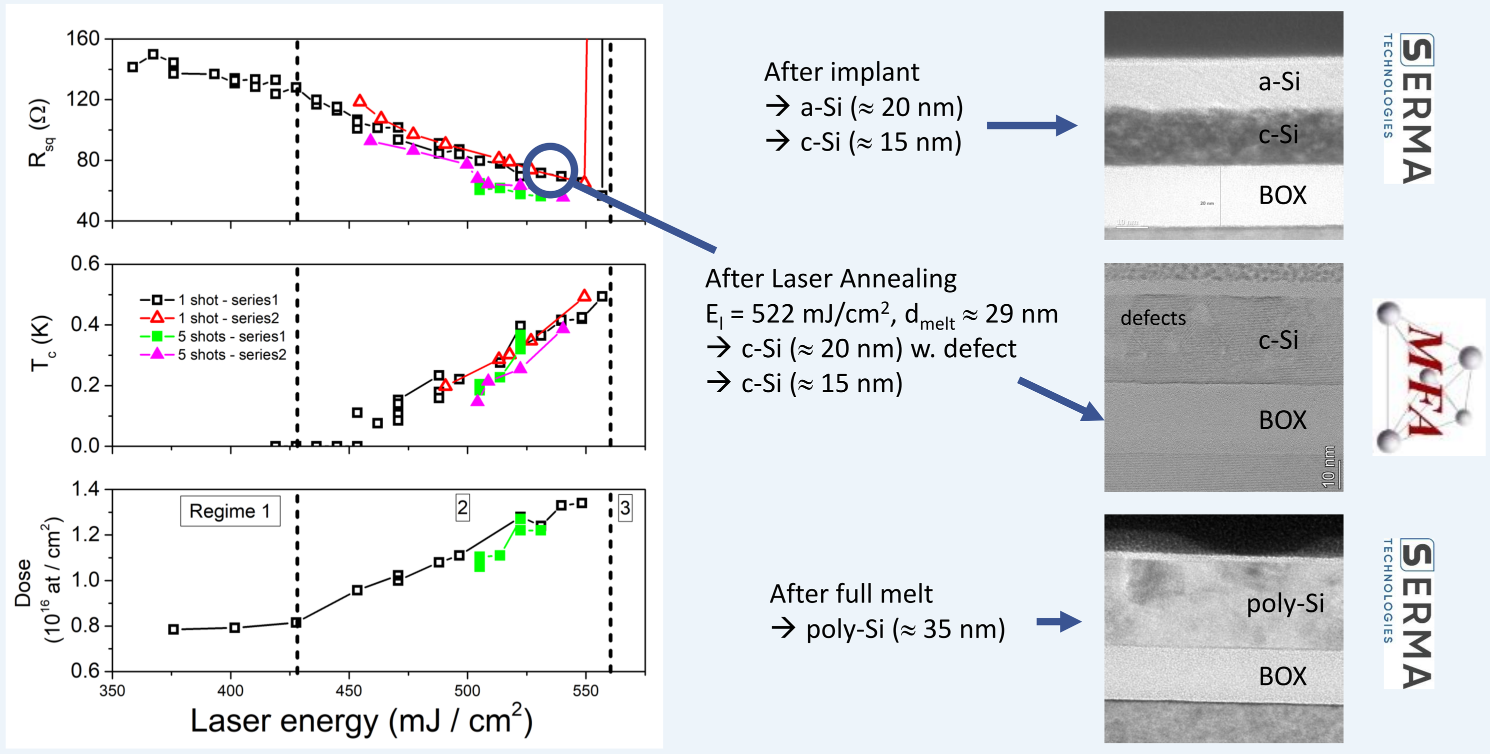


The TEM images shows good conformal deposition in large and small structures with a pre-formation of a Co_xSi_{1-x} layer at the Co-Si interface.

Boron doped SOI epilayers

→ Nanosecond Pulsed Laser Annealing





Combining ultra high boron implantation and laser annealing, we can generate superconducting silicon epilayer with Tc up to 0.5 K

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