SuperLink

Superconducting quantum-classical linked computing systems

Abstract

SuperLink aims at tackling critical open problems in quantum computing with superconducting qubits. Superconducting qubits are leading candidates for scaling to disruptively useful quantum computations. However, it has become clear that scaling beyond 100 qubits will require dramatically different architectures. Our goal is to develop fundamentally new resources to facilitate the scaling up of superconducting quantum computing while reducing the number of input/output channels with novel multiplexing approaches. Integrated circuits based on superconducting single-flux quantum (SFQ) digital logic will be designed, tested, and then integrated with quantum circuits [1 - 4]. We propose a hybrid of classical superconducting SFQ electronics, packaged and linked to quantum devices. Such novel quantum resources developed by SuperLink will represent a decisive step forward in the realization of superconducting quantum processors with a truly scalable architecture.

Consortium

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In strong collaboration with SeeQC company

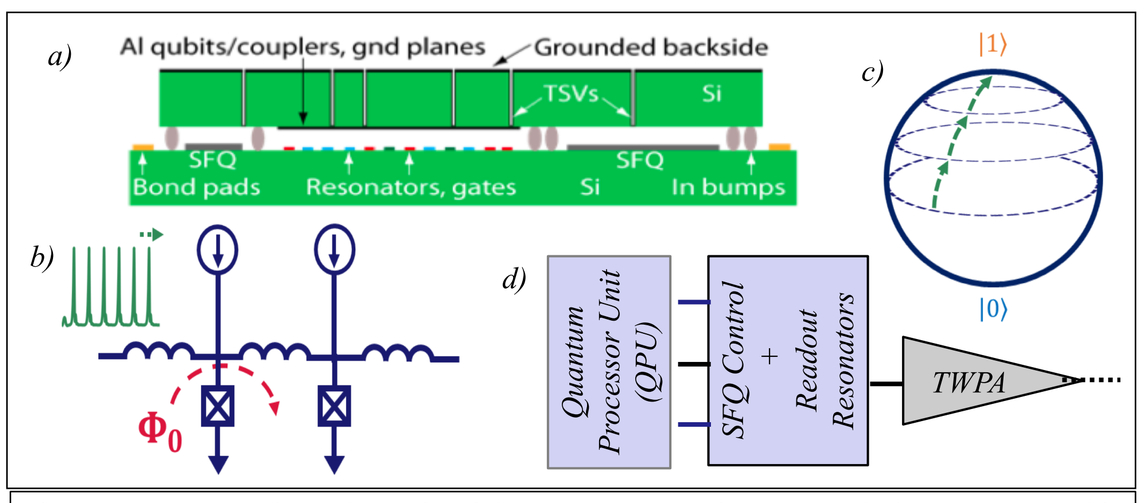


Fig 1: (a) Cross-section schematic of the multi-chip-module MCM design. Quantum chip above and control chip below [1, 2]. (b) Schematic of a typical single flux quantum (SFQ) digital circuit, where (green) quantized pulses move along a superconducting circuit composed of Josephson junctions (blue crossed squares) [3]. (c) Representation on the Bloch sphere of a qubit irradiated by a train of SFQ pulses for digital control. (d) Setup sketch for quantum-noise-limited multiplexed readout of qubits located on the Quantum Processor Unit (QPU) via a Josephson Traveling Wave Parametric Amplifier (TWPA) in combination with SFQ digital control.

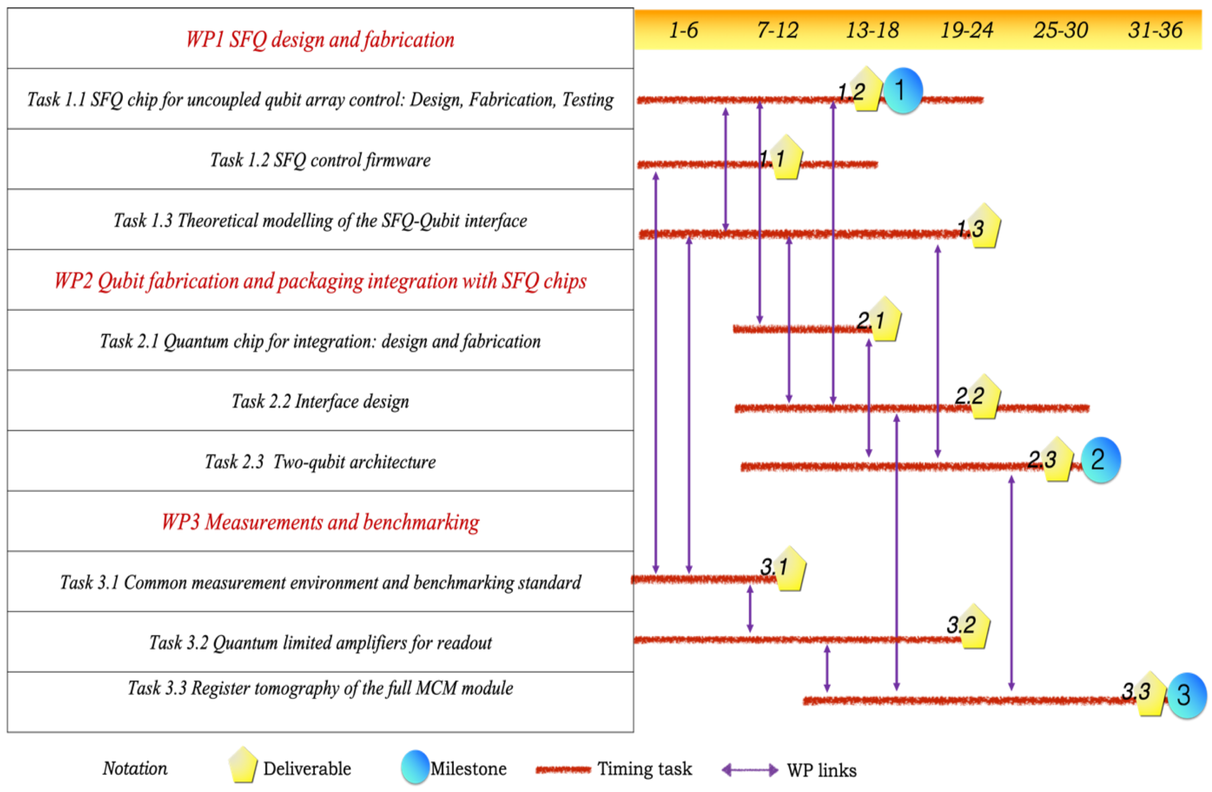
References

[1] Opremcak et al. Science 361, 6408 (2018)
[2] Govia et al. Phys. Rev. A 90, 062307 (2014)
[3] O. Mukhanov, IEEE Trans. Appl. Supercond. 3, 2578-2581 (1993)
[4] Kangbo Li et al., Phys. Rev. Applied 12, 014044 (2019)

Objectives and milestones:

- Design and experimental validation of SFQ control for a qubit array.
- Design and realization of quantum chips and their integration with SFQ control chips for hardware efficient optimal control.
- SFQ control of 10 qubit register benchmarked.

Workplan



WP1: SFQ design and fabrication

WP1 deals with scalable SFQ digital circuits to implement high fidelity control of multi-qubit quantum arrays [1,2]: design, fabrication and of SFQ drivers [3] and SFQ qubit controller chips for multi chip module (MCM) integration.

Deliverables:

D2.1 Report on the design and fabrication of the Q chip adapted to the flip-chip MCM environment;
D2.2 Report on 3D integration designs;
D2.3 Report detailing 2-qubit gate optimized 10-qubit architecture.

WP2: Qubit fabrication and packaging integration with SFQ chips

WP2 efforts are focussed on the design and fabrication of the quantum (Q) chip, thus evaluating different qubit and coupler designs together with their respective control units. The developed Q chip will be integrated into an optimised MCM architecture [2,4].

Deliverables:

D1.1 Full set of coherence-adapted design rules for SFQ circuits;
D1.2 Experimental demonstration of SFQ controller circuit for qubit control;
D1.3 Gate fidelity optimization for a two-qubit gate

WP3: Measurements and benchmarking

The objective of WP3 is to provide quantum measurement, verification and benchmarking of the complete MCM packages. We will apply the control and optimization techniques to achieve >99.0% fidelity on both single-qubit and two-qubit gates. Multiplexed readout via travelling wave amplifiers will provide <1% error in <100 nsec on the full qubit register.

Deliverables:

D3.1 Report on MCM measurement from all measurement sites;
D3.2 Report on system fidelities (expect >99% for both single and two-qubit gates);
D3.3 Report on full 10 qubit register measurement (with SFQ control and multiplexed microwave readout).

	SuperLink approach	Standard approach
Controlling signals to qubit	Digital pulse pattern	Analog microwave waveforms
Clock speed	20-40 GHz	0.2-2 GHz
Power dissipation for qubit control	0.0002 mW/qubit	20 mW/qubit (now) 2 mW (potential with cryoCMOS)
Heating from cables	Limits 1M-100M qubits	Limits to 100-150 qubits (360 qubits optimistically)
Interference	Low	High
Cost	100 Euro/qubit up 50 qubit processor <10 Euro/qubit for >50 qubit processor	10000 Euro/qubit (linear scale)